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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,002	01/15/2002	Mark Pavier	IR-1837	5495

2352 7590 09/24/2003

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EXAMINER	
CHU, CHRIS C	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/050,002	PAVIER, MARK	
	Examin r	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12 - 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12 - 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. Applicant's amendment filed on July 7, 2003 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitations in claim 1 "a first semiconductor die having ... a first major electrode of a first functionality disposed on a first major surface thereof" and "a second semiconductor die having ... a first major electrode of a first functionality disposed on a first major surface thereof" and the limitation in claim 18, "all electrical connections are made by wires" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Applicant argues "a detailed illustration is not essential for a proper understanding of the invention ... Applicant respectfully requests that the Examiner withdraw the objection." Applicant request to withdrawn the drawing objection is fully considered but not persuasive because "not essential" is not equivalent to conventional. Since both sides of the semiconductor chip having electrodes and all electrical connections being made by wires are claimed, applicant is required to show this feature in the drawings.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golwalkar et al. in view of Kim.

Regarding claim 12, Golwalkar et al. discloses in Fig. 1 and Fig. 10 a semiconductor device comprising:

- a lead frame (20), said lead frame including a conductive die pad (25) having a first major surface and a second major surface opposing said first major surface, and a first plurality of leads (46) disposed at a first edge of said conductive die pad and a second plurality of leads (44) disposed at a second edge of said conductive die pad, said second edge of said conductive die pad being opposite to said first edge of said conductive die pad;
- a first semiconductor die (50) having a second major electrode of a second functionality disposed on a second opposing major surface thereof;
- a second semiconductor die (90) having a second major electrode of a second functionality disposed on a second opposing major surface thereof;
- a molded housing (66) encapsulating said conductive die pad, said first semiconductor die, said second semiconductor die, and portions of said first plurality of leads and said second plurality of lead; and
- wherein said second major electrode of said first semiconductor die and said second major electrode of said second semiconductor die are electrically connected to said first plurality of leads.

Golwalkar et al. does not disclose a first semiconductor die having a first major electrode of a first functionality disposed on a first major surface thereof and said first major electrode of said first semiconductor die being electrically connected to said first major surface of said conductive die pad; a second semiconductor die having a first major electrode of a first functionality disposed on a first major surface thereof and said first major electrode of said second semiconductor die being electrically connected to said second major surface of said

conductive die pad; and wherein said conductive die pad is electrically connected to at least one of said second plurality of leads. However, Kim discloses in Fig. 2 a first semiconductor die (22) having a first major electrode (electrodes under 22) of a first functionality disposed on a first major surface thereof and the first major electrode of the first semiconductor die being electrically connected to a first major surface of a conductive die pad (a structure under 21); a second semiconductor die (23) having a first major electrode (electrodes on top of 23) of a first functionality disposed on a first major surface thereof and the first major electrode of the second semiconductor die being electrically connected to a second major surface of the conductive die pad; and wherein the conductive die pad is electrically connected (25) to at least one of the second plurality of leads (24, at the right). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Golwalkar et al. by using the first major electrodes of the first and second semiconductor dice and the electrical connections of the conductive die pad as taught by Kim. The ordinary artisan would have been motivated to modify Golwalkar et al. in the manner described above for at least the purpose of providing an easy bonding and mass production (column 5, lines 51 ~ 54).

Further, the limitation "whereby ..." has been held that the functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish. In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).

Regarding claim 15, Golwalkar et al. discloses in Fig. 8 the first plurality of leads including four spaced leads, and said second plurality of leads including four spaced leads.

Regarding claim 19, Golwalkar et al. discloses in Fig. 10 said first plurality of leads being spaced from said conductive die pad and said second plurality of leads being spaced from said conductive die pad.

6. Claims 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golwalkar et al. and Kim as applied to claim 12 above, and further in view of Munoz et al.

Regarding claim 13, Golwalkar et al. and Kim disclose the claimed invention except for at least one of said semiconductor die being MOSFET. Munoz et al. discloses in column 2, lines 31 and 32 a semiconductor die being MOSFET. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Golwalkar et al. by using the MOSFET to the first and second semiconductor dice as taught by Munoz et al. The ordinary artisan would have been motivated to further modify Golwalkar et al. in the manner described above for at least the purpose of providing the simultaneous formation of the necessary junctions (column 1, lines 8 ~ 16).

Regarding claim 14, Golwalkar et al. and Kim disclose the claimed invention except for the first and second semiconductor dice including a control electrode on said second major surface thereof. Munoz et al. discloses in Fig. 2 and column 2, lines 31 ~ 41 a control electrode (12) on the second major surface of a semiconductor die (10). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Golwalkar et al. by using the control electrode on the second major surface of the first and second semiconductor dice as taught by Munoz et al. The ordinary artisan would have been

motivated to further modify Golwalkar et al. in the manner described above for at least the purpose of increasing an area of a package (column 2, lines 50 ~ 51).

Regarding claim 16, Golwalkar et al. and Kim disclose the claimed invention except for the first major electrode being a drain electrode of a MOSFET die and the second major electrode being a source electrode of a MOSFET die. Munoz et al. discloses in Fig. 2 and column 2, lines 31 ~ 41 a first major electrode (13) being a drain electrode of a MOSFET die and the second major electrode being a source electrode (11) of a MOSFET die. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Golwalkar et al. by using the drain electrode and the source electrode of a MOSFET die as taught by Munoz et al. The ordinary artisan would have been motivated to further modify Golwalkar et al. in the manner described above for at least the purpose of providing the simultaneous formation of the necessary junctions (column 1, lines 8 ~ 16).

7. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golwalkar et al., Kim and Munoz et al. as applied to claims 12 ~ 14 above, and further in view of Adishian.

Regarding claim 17, Golwalkar et al., Kim and Munoz et al. discloses in Fig. 2 and column 2, lines 31 ~ 41 each of the semiconductor die being a MOSFET, said control electrode being a gate electrode (12), said first major electrode being a drain electrode (13), and said second major electrode being a source electrode (11). However, Golwalkar et al., Kim and Munoz et al. does not disclose said gate electrodes of said MOSFETs being electrically connected to one of said plurality of second leads, said source electrodes of said MOSFETs

being electrically connected to another one of said second plurality of leads, and said conductive die pad being electrically connected to the remaining leads of said second plurality of leads, and the source electrodes of said MOSFETs being also connected to said first plurality of leads. Adishian discloses in Fig. 1 ~ Fig. 5 and column 2, line 37 the gate electrodes (G1, G2, etc.) of the MOSFETs being electrically connected to one of the plurality of second leads (24), the source electrodes (S1, S2, R1, R2, etc.) of the MOSFETs being electrically connected to another one of the second plurality of leads (22), and the conductive die pad (12) being electrically connected to the remaining leads of the second plurality of leads (GA, GB, and GC), and the source electrodes of the MOSFETs being also connected to the first plurality of leads. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Golwalkar et al. by using the connections between the electrodes and the leads as taught by Adishian. The ordinary artisan would have been motivated to further modify Golwalkar et al. in the manner described above for at least the purpose of providing a structurally, both thermally and electrically optimized and improved very-high-power transistor (column 1, lines 56 ~ 61).

Regarding claim 18, Golwalkar et al. and Kim discloses all electrical connections being made by wires.

Response to Arguments

8. Applicant's arguments filed on July 7, 2003 have been fully considered but they are not persuasive.

On page 7, applicant argues "Kim does not teach use of a die pad. Instead, Kim teaches flip chip bonding between a semiconductor chip and an interface board, which is a printed circuit board (PCB)." This argument is not persuasive since it attempts to distinguish the claim from Golwalkar et al. and Kim merely through semantics. Whether one refers to an element (21) as a die pad or an interface board, there is no structural or functional difference.

Further, applicant argues "if the interface board of Kim were a conductive die pad, as that term is known in the art, then the device shown in Fig. 2 is non-functional." This argument is not persuasive because the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Even further, applicant argues "neither Golwalkar et al. nor Kim teaches a first semiconductor die having a first major electrode of a first functionality and a second semiconductor die having a first major electrode of a first functionality, said first major electrode of said first semiconductor die and said first major electrode of the second semiconductor die being electrically connected to said first major surface of said conductive die pad." This argument is not persuasive. Kim teaches in Fig. 2 a first semiconductor die (22) having a first major electrode (electrodes under 22) of a first functionality and a second semiconductor die (23) having a first major electrode (electrodes on top of 23) of a first functionality, said first major

electrode of said first semiconductor die and said first major electrode of the second semiconductor die being electrically connected to said first major surface of said conductive die pad. Thus, a combined structure of Golwalkar et al. and Kim teaches each and every element of the invention; therefore, the combination establishes prima facie obviousness under 35 USC § 103.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Contrary to applicant's assertion and as stated in the rejection, motivation was established by Kim, specifically in column 5, lines 51 ~ 54 (providing an easy bonding and mass production).

For the above reasons, the rejection is maintained.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800